In the Claims:

Claims 1-12 (Cancelled).

13. (Currently Amended) A decoding circuit for decoding a biphase signal having a pair of states and comprising:

a precharging register for precharging respective ~~the~~ states of the biphase signal, one state of the pair of states being precharged at each pulse of a periodic precharging signal; and

a verification circuit cooperating with said precharging register for comparing the two states of the pair of states to detect an error and providing an error signal when the two states are equal indicating that they have not been received accurately.

Claims 14 and 15 (Cancelled).

16. (Currently Amended) The decoding circuit of ~~Claim 15~~ Claim 13 further comprising a storage circuit for storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

17. (Previously presented) The decoding circuit of Claim 13 further comprising a delay circuit connected to said verification circuit and providing an end signal indicating an end of the biphase signal after a predetermined delay, said delay

circuit being initialized at the beginning of the biphase signal.

18. (Previously presented) The decoding circuit of Claim 13 further comprising a filter upstream from said precharging register for filtering the biphase signal.

19. (Currently Amended) A decoding circuit for decoding a biphase signal having a pair of states representing a value, the decoding circuit comprising:

a precharging register for precharging respective ~~the~~ states of the biphase signal, one state of the pair of states being precharged at each pulse of a periodic precharging signal; and

a verification circuit cooperating with said precharging register for comparing the two states of the pair of states and providing an error signal when the two states are equal indicating that they have not been received accurately, said verification circuit also providing a decoded signal indicating the value of the precharged pair of states.

20. (Previously presented) The decoding circuit of Claim 19 further comprising a storage circuit for storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

21. (Previously presented) The decoding circuit of

Claim 19 further comprising a delay circuit connected to said verification circuit and providing an end signal indicating an end of the biphase signal after a predetermined delay, said delay circuit being initialized at the beginning of the biphase signal.

22. (Previously presented) The decoding circuit of Claim 19 further comprising a filter upstream from said precharging register for filtering the biphase signal.

23. (Previously presented) A circuit for transmitting and receiving biphase signals having respective pairs of states and comprising:

transmission and reception circuitry for sending and receiving the biphase signals; and

a decoding circuit coupled to said reception circuitry for decoding the biphase signals and comprising

a precharging register for precharging respective states of the biphase signals, one state of each pair of states being precharged at each pulse of a periodic precharging signal; and

a verification circuit for comparing the two states of each pair of states to detect an error and providing an error signal when the two states are equal indicating that they have not been received accurately.

24. (Previously presented) The circuit of Claim 23 wherein the biphase signals are encoded according to the digital

addressable lighting interface (DALI) communications protocol.

Claim 25 (Cancelled).

26. (Previously presented) The circuit of Claim 23 wherein the pair of states represent a value, and wherein said verification circuit also provides a decoded signal indicating the value of each precharged pair of states.

27 (Previously presented) The circuit of Claim 26 wherein said decoding circuit further comprises a storage circuit for storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

28. (Previously presented) The circuit of Claim 23 wherein said decoding circuit further comprises a delay circuit connected to said verification circuit and providing an end signal indicating an end of each biphase signal after a predetermined delay, said delay circuit being initialized at the beginning of each biphase signal.

29. (Previously presented) The circuit of Claim 23 wherein said decoding circuit further comprises a filter upstream from said precharging register for filtering the biphase signals.

30. (Previously presented) A method for decoding a

biphase signal having a pair of states, the method comprising:

precharging one of the pair of states of the biphase signal into a precharging register at each pulse of a periodic precharging signal;

comparing the two states of the precharged pair of states to detect an error when the two states are equal indicating that they have not been received accurately; and

providing an error signal based upon detecting the error.

Claim 31 (Cancelled).

32. (Previously presented) The method of Claim 30 further comprising supplying a decoded signal indicating a value of the precharged pair of states.

33. (Previously presented) The method of Claim 32 further comprising storing the decoded signal at each pulse of a periodic validation signal, the periodic validation signal having a period equal to twice the period of the periodic precharging signal.

34. (Previously presented) The method of Claim 30 further comprising measuring a predetermined time from a start of the biphase signal, and providing an end signal after the predetermined time indicating an end of the biphase signal.

35. (Previously presented) The method of Claim 30 further comprising filtering the biphase signal prior to precharging each of the pair of states.